Set	Items	Description
S1	5	((1 OR ONE OR 1ST OR FIRST)()HOT)(2W)(VECTOR? ? OR TAG? ? - OR FLAG? ? OR INDICATOR? ?)
S2	12182	(1 OR ONE OR 1ST OR FIRST)(2N)VECTOR? ?
S3	17213	(N(1W)1 OR N()MINUS()(1 OR ONE))(3W)(ZERO?? OR O OR 0 OR OS OR OS)
S4	3	((2 OR TWO OR 2ND OR SECOND???)()HOT)(2W)(VECTOR? ? OR TAG? ? OR FLAG? ? OR INDICATOR? ?)
S5	14259	(2 OR TWO OR 2ND OR SECOND??)(2N)VECTOR? ?
S6	15269	(N(1W)2 OR N()MINUS()(2 OR TWO))(3W)(ZERO?? OR O OR 0 OR OS OR OS)
S7	570	(NBIT OR N()BIT)(2W)(STRING? ? OR BLOCK? ? OR FRAGMENT? ? - OR WORD? ? OR STATEMENT? ?)
S8	53506	TAG? ? OR TLB OR TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()- BUFFER? ? OR CACH???
S9	398	S1:S3(10N)S4:S6(10N)(CONVERT??? OR CONVERSION? ? OR TRANSF- ORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATION? ? OR MODIF?)
S10	16	S7:S8 AND S9
S11	3	S1 AND S4:S6
S12	3	S4 AND S1:S3
S13	335	S2(7N)S5(7N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATI- ON? ? OR MODIF?)
S14	7	S3(7N)S6(7N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATI- ON? ? OR MODIF?)
S15	25	S10:S12 OR S14

06261619   **Image available**
CACHE MEMORY

PUB. NO.:   11-203199 [JP 11203199 A]
PUBLISHED: July 30, 1999 (19990730)
INVENTOR(s):   NAFFZIGER SAMUEL D
APPLICANT(s):   HEWLETT PACKARD CO <HP>
APPL. NO.:   10-300695 [JP 98300695]
FILED: October 22, 1998 (19981022)
PRIORITY: 955821 [US 955821], US (United States of America), October
                22, 1997 (19971022)
INTL CLASS: G06F-012/08; G06F-012/10

ABSTRACT
PROBLEM TO BE SOLVED: To shorten a access time in a **cache** memory by
comparing first and second vectors in a digital comparator and selecting
data from a second memory structure by utilizing a compared result.

SOLUTION: The first vector indicating a position inside a **translation**
lookaside buffer 210 including the position matching with a virtual tag is
generated by a **translation** lookaside buffer 210. At least **one second
vector** indicating whether or not a **tag** matched with a physical **tag** is
housed at least one position inside the **translation lookaside buffer**
210 is retrieved from at least one position decided by a virtual index by a
first memory structure 204. Then, by the digital comparator 216, the **first
vector** and the **second vector** are compared. By utilizing the compared
result, the data are selected from the second memory structure 106. Thus,
the access time in this **cache** memory is shortened.

02811218   **Image available**
ERROR CORRECTION CODING METHOD

PUB. NO.:   01-108818 [JP 1108818 A]
PUBLISHED: April 26, 1989 (19890426)
INVENTOR(s):   KUME ATSUYA
APPLICANT(s):   MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
                Corporation), JP (Japan)
APPL. NO.:   62-267151 [JP 87267151]
FILED: October 21, 1987 (19871021)
INTL CLASS: [4] H03M-013/00
JAPIO CLASS: 42.4 (ELECTRONICS -- Basic Circuits)
JOURNAL: Section: E, Section No. 800, Vol. 13, No. 350, Pg. 5, August
                07, 1989 (19890807)

ABSTRACT
PURPOSE: To improve the transmission quality by changing the error
correction capability in response to the importance of data so as to
improve the error correction capability.

CONSTITUTION: Data D to be sent (supposing data being an analog quantity
quantized by an n-bit binary number) is inputted in series with an input
terminal 1, led to a data distributer 2, where the data is **converted** in
parallel and data $2(\sup n - 1) - 2(\sup 0)$ of each digit are given to
corresponding coders 3(n-1)-30. An error correction code having a higher
error correction capability than that of the coder 3(n-2) is provided to
the coder 3(n-1) with respect to the inputted data and the data of the
least significant data is coded by the error correction code having a

smaller error correction capability than that of the coder 30 sequentially as above. The coded n-set of data is converted into a serial data by a data synthesizer 4. Thus, the transmission quality is enhanced.

15/5/3   (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

01907474   **Image available**
VIDEO SIGNAL PROCESSING CIRCUIT

PUB. NO.:   61-121574 [JP 61121574 A]
PUBLISHED: June 09, 1986 (19860609)
INVENTOR(s):   NODA MASARU
                KATO MINORU
APPLICANT(s):   HITACHI LTD [000510] (A Japanese Company or Corporation), JP
                (Japan)
APPL. NO.:   59-242310 [JP 84242310]
FILED: November 19, 1984 (19841119)
INTL CLASS: [4] H04N-005/205
JAPIO CLASS: 44.6 (COMMUNICATION -- Television)
JOURNAL: Section: E, Section No. 447, Vol. 10, No. 309, Pg. 50,
                October 21, 1986 (19861021)

ABSTRACT

PURPOSE: To set optionally a comb-shaped characteristic by a feedback ratio K and to improve an S/N while the response is zero by setting an adding ratio A to a special relation shown by a primary function concerning the feedback ratio K.

CONSTITUTION: An output signal of a vertical outline extracting comb-shaped filter 10 is injected through an adding coefficient circuit 7 to an adder circuit 8, and here, added with an input video signal and the desired output video signal is obtained at an output terminal 2, and when the adding coefficient circuit 7 is a straight line characteristic, a communicating characteristic G2 from an input terminal 7 to an output terminal 2 is shown by a formula. Here, an adding coefficient A is set to a special relation for a feedback ratio K, the item 1 of the product of the formula means an adding average of a 1H delaying signal and a non-delaying signal and shows a comb-shaped characteris tic in which the response at $f=(n+1/2)$ fH goes to **zero** . The response at $f=(n+1/2)$ fH is **zero** regardless of the K value. The comb-shaped characteristic can be **changed** by the value of the feedback ratio K, for example, as the setting of K=0.75, the response can be reduced over the wide band with $f=(n+1/2)$ fH as a center, and large S/N improving effects can be obtained.

15/5/5   (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

016216435   **Image available**
WPI Acc No: 2004-374323/200435
Related WPI Acc No: 2002-665572; 2003-864414
XRPX Acc No: N04-297793
    Tag **array memory for** cache **memory, converts received 1-** hot   vector
    to 2-hot vector, stores 2-hot vector in memory array and converts 2-hot
    vector back to 1 - hot   vector
Patent Assignee: INTEL CORP (ITLC)
Inventor: CRAWFORD J H; GROCHOWSKI E; KOSARAJU C; MATHEWS G S; QUACH N T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040078529	A1	20040422	US 2000750094	A	20001229	200435	B
			US 2003435386	A	20030512		
			US 2003726492	A	20031204		

Priority Applications (No Type Date): US 2000750094 A 20001229; US
  2003435386 A 20030512; US 2003726492 A 20031204
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20040078529 A1   14 G06F-012/08   Div ex application US 2000750094
                                      Div ex application US 2003435386
                                      Div ex patent US 6675266

Abstract (Basic): US 20040078529 A1
        NOVELTY - The memory includes an input **conversion** circuit which
   receives 1-hot vector (112) and converts the 1-hot vector to 2-hot
   vector. A memory array coupled to the input conversion circuit, stores
   the 2-hot vector, while an output conversion circuit coupled to the
   memory array, receives the 2- **hot   vector** and converts the **2 - hot
   vector** back to the **1 - hot   vector** .
        DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the
   following:
        (1) computer system;
        (2) **1 - hot   vectors   cache** protection method; and
        (3) recorded medium storing **1 - hot   vectors** protection program.
        USE - **Tag** array memory for use in high performance microprocessor
   and multi-processor-based personal computer system.
        ADVANTAGE - Protects the **1 - hot   vectors** used in the **tag**
   array, while providing hardware savings. Also, it operates at high
   speeds and is easy to implement.
        DESCRIPTION OF DRAWING(S) - The figure shows a logic block diagram
   of the **2 - hot   tag   cache** based on the **1 - hot   tag   cache** .
        tag (102)
        translation   look - aside   buffer (**TLB**) (1109)
        TLB virtual address array (110)
        1 - hot   vector (112)
        1 - hot   tag array (120)
        2 - hot   tag   cache (419)
        1 - hot   vector block (422)
        pp; 14 DwgNo 4/7
Title Terms: **TAG** ; ARRAY; MEMORY; **CACHE** ; MEMORY; CONVERT; RECEIVE; HOT;
  VECTOR; HOT; VECTOR; STORAGE; HOT; VECTOR; MEMORY; ARRAY; CONVERT; HOT;
  VECTOR; BACK; HOT; VECTOR
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

 15/5/8   (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015802211   **Image available**
WPI Acc No: 2003-864414/200380
Related WPI Acc No: 2002-665572; 2004-374323
XRPX Acc No: N03-690026
  **Tag array memory for multiprocessor, accesses memory bits simultaneously
  when** 1 - hot   vector **stored in memory bit is valid**
Patent Assignee: INTEL CORP (ITLC)
Inventor: CRAWFORD J; GROCHOWSKI E; KOSARAJU C; MATHEWS G S; QUACH N
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
US 20030196049 A1   20031016 US 2000750094 A   20001229 200380 B
                               US 2003435386 A   20030512

Priority Applications (No Type Date): US 2000750094 A 20001229; US
  2003435386 A 20030512
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030196049 A1   15 G06F-012/00   Div ex application US 2000750094

Abstract (Basic): US 20030196049 A1

NOVELTY - The valid bit circuit coupled to the n-bit memory cell accesses the memory bits simultaneously when the **1 - hot   vector** stored in the memory bit is valid.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) **1 - hot   vector** protection method;

(2) recording medium storing the **1 - hot   vector** protection program; and

(3) computer system.

USE - For multiprocessor or computer system (claimed).

ADVANTAGE - The operating speed is increased by simple construction and vectors used in tag array saves space in designed hardware.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the **2 - hot   tag** cache.

index (104)

comparators (130-133)

multiplexers (140,150)

tag array (420)

hot vector block (422)

pp; 15 DwgNo 4/7

Title Terms: TAG; ARRAY; MEMORY; MULTIPROCESSOR; ACCESS; MEMORY; BIT; SIMULTANEOUS; HOT; VECTOR; STORAGE; MEMORY; BIT; VALID

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

15/5/13   (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014844866   **Image available**

WPI Acc No: 2002-665572/200271

Related WPI Acc No: 2003-864414; 2004-374323

XRPX Acc No: N02-526548

Tag array memory circuit for cache memory, comprises valid bit circuit which is set to valid, when valid hot vector is stored in memory bit circuits

Patent Assignee: CRAWFORD J (CRAW-I); GROCHOWSKI E (GROC-I); KOSARAJU C (KOSA-I); MATHEWS G S (MATH-I); QUACH N (QUAC-I); INTEL CORP (ITLC)

Inventor: CRAWFORD J; GROCHOWSKI E; KOSARAJU C; MATHEWS G S; QUACH N

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020087808	A1	20020704	US 2000750094	A	20001229	200271	B
US 6675266	B2	20040106	US 2000750094	A	20001229	200411	

Priority Applications (No Type Date): US 2000750094 A 20001229

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020087808	A1		15	G06F-012/00	
US 6675266	B2			G06F-012/00	

Abstract (Basic): US 20020087808 A1

NOVELTY - Several memory bit circuits are connected together to form a n-bit memory cell, to which a valid bit circuit is connected. The valid bit circuit is set to valid or invalid, based on the valid or invalid hot vector (112) stored in the memory bit circuits. The valid bit and memory bit circuits are accessed simultaneously.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) **Vectors** protection method;

(2) Machine readable medium storing vectors protection program;

(3) Tag array memory; and

(4) Computer system.

USE - For high speed on chip memory buffer such as cache used in high performance 32,64 model processor.

ADVANTAGE - Minimizes global routing at the expense of local

interconnections. Provides highly reliable high performance microprocessor with simplified design.

DESCRIPTION OF DRAWING(S) - The figure shows the logic block diagram of a **2** - **hot** **tag** cache based on the **1** - **hot** **tag** cache.

Hot vector (112)

pp; 15 DwgNo 4/7

Set	Items	Description
S1	14	((1 OR ONE OR 1ST OR FIRST)()HOT)(2W)(VECTOR? ? OR TAG? ? - OR FLAG? ? OR INDICATOR? ?)
S2	39242	(1 OR ONE OR 1ST OR FIRST)(2N)VECTOR? ?
S3	42126	(N(1W)1 OR N()MINUS()(1 OR ONE))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S4	1	((2 OR TWO OR 2ND OR SECOND???)()HOT)(2W)(VECTOR? ? OR TAG? ? OR FLAG? ? OR INDICATOR? ?)
S5	26322	(2 OR TWO OR 2ND OR SECOND??)(2N)VECTOR? ?
S6	32891	(N(1W)2 OR N()MINUS()(2 OR TWO))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S7	994	(NBIT OR N()BIT)(2W)(STRING? ? OR BLOCK? ? OR FRAGMENT? ? - OR WORD? ? OR STATEMENT? ?)
S8	112819	TAG? ? OR TLB OR TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()- BUFFER? ? OR CACH???
S9	1585	S1:S3(10N)S4:S6(10N)(CONVERT??? OR CONVERSION? ? OR TRANSF- ORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATION? ? OR MODIF?)
S10	358	S1:S3(10N)S4:S6(10N)(MODIF???? OR MODIFICATION)
S11	78	S9:S10(50N)S7:S8
S12	1	S1(20N)S4:S6
S13	1033	S2(7N)S5(7N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATI- ON? ? OR MODIF???? OR MODIFICATION)
S14	212	S3(7N)S6(7N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATI- ON? ? OR MODIF???? OR MODIFICATION)
S15	79	S11:S12

DIALOG(R)File 348:EUROPEAN PATENTS

01017398
Cache memory with reduced access time
Cachespeicher mit verminderter Zugriffszeit
Antememoire a temps d'acces reduit
PATENT ASSIGNEE:
  Hewlett-Packard Company, (206030), 3000 Hanover Street, Palo Alto,
    California 94304, (US), (applicant designated states:
    AT;BE;CH;CY;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
  Naffziger, Samuel D., 3749 Ashmount Dr., Fort Collins, CO 80525, (US)
LEGAL REPRESENTATIVE:
  Schoppe, Fritz, Dipl.-Ing. (55463), Schoppe & Zimmermann Patentanwalte
    Postfach 71 08 67, 81458 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 911737 A1 990428 (Basic)
APPLICATION (CC, No, Date):   EP 98108916 980515;
PRIORITY (CC, No, Date): US 955821 971022
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-012/10;
ABSTRACT WORD COUNT: 224

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9917	410
SPEC A	(English)	9917	2879
Total word count - document A			3289
Total word count - document B			0
Total word count - documents A + B			3289

...CLAIMS physical tag (203) separate from the virtual address;
  generating a first vector (214), by a **translation** lookaside buffer
    (210), indicating a location in the translation lookaside buffer that
    contains a match...

...structure (204), from at least one location determined by the virtual
    index, at least one **second** **vector** , the **second** **vector**
    indicating whether at least one location in the **translation**
    lookaside **buffer** contains a **tag** that matches the physical **tag** ;

comparing, by a digital comparator (216), the **first** **vector** and the
  second **vector** ; and
using the result of comparing to select data from a second memory
  structure (106...
...virtual address (200) comprising index bits (102) and tag bits (202),
  the cache comprising:
  a **translation** -lookaside buffer (210), the translation lookaside buffer
    receiving the tag bits and generating a first...

...tag bits;
  a memory structure (204), receiving the index bits, the memory structure
    containing second **vectors** , each **second** **vector** indicating at
    least one location of a physical address tag in the **translation**
    lookaside buffer, at least **one** **second** **vector** designated by the
    index bits;
  at least **one** **vector** comparator (216) comparing the **second** **vector**
    from the memory structure to the **first** **vector** from the
    translation lookaside buffer.
  4. The cache of claim 3, the virtual address further comprising page
    offset bits (222), the **cache** further comprising:
  a second memory structure (220), receiving the index bits, the second
    memory structure...

00846256
Determination of array padding using collision vectors
Ermittlung von Polstern zwischen Feldern mittels Kollisionsvektoren
Determination de coussinage entre champs utilisant des vecteurs de collision
PATENT ASSIGNEE:
    SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View,
        California 94043-1100, (US), (Proprietor designated states: all)
INVENTOR:
    Wallace, David R., 1677 Cornell Drive, Mountain View, California
        94043-1100, (US)
    Oblock, Gary, 1960 Jones Street, San Francisco, California 94133, (US)
LEGAL REPRESENTATIVE:
    Browne, Robin Forsythe, Dr. (55142), Urquhart-Dykes & Lord Tower House
        Merrion Way, Leeds LS2 8PA, (GB)
PATENT (CC, No, Kind, Date):   EP 782078   A2   970702 (Basic)
                               EP 782078   A3   980708
                               EP 782078   B1   020313
APPLICATION (CC, No, Date):   EP 96308973 961211;
PRIORITY (CC, No, Date): US 579435 951227
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G06F-012/08
ABSTRACT WORD COUNT: 152
NOTE:
    Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text   Language   Update   Word Count
        CLAIMS A (English) EPAB97   1528
        CLAIMS B (English) 200211   1361
        CLAIMS B (German)   200211   1229
        CLAIMS B (French)   200211   1596
        SPEC A   (English) EPAB97   6174
        SPEC B   (English) 200211   6111
Total word count - document A   7704
Total word count - document B   10297
Total word count - documents A + B   18001

...SPECIFICATION An expanded interval for the first dimension of (-11, +11)
    is used which reflects the **cache** line size of 8 plus additional offsets
    introduced by software pipelining (which effectively increases the range
    of the offsets in the first dimension).
    Applying these ranges to the collision **vector** (1 , - 2 , 0) yields
    digit ranges of the form ((-10, 12), (-4, 0)) in base 257 arithmetic.
    These ranges are then **translated** to decimal form. In this case that
    leaves 1(+-)11, -256(+-)11, -513(+-)11, -770...

...245), (-524, -502), (-781, -759), (-1038, -1016)). Negative range
    offsets are then adjusted modulo the **cache** size, giving the set of
    interval ranges to be avoided: ((65525, 65535), (0, 12), (65269...

...SPECIFICATION An expanded interval for the first dimension of (-11, +11)
    is used which reflects the **cache** line size of 8 plus additional offsets
    introduced by software pipelining (which effectively increases the range
    of the offsets in the first dimension).
    Applying these ranges to the collision **vector** (1 , - 2 , 0) yields
    digit ranges of the form ((-10, 12), (-4, 0)) in base 257 arithmetic.
    These ranges are then **translated** to decimal form. In this case that
    leaves 1(+-)11, -256(+-)11, -513(+-)11, -770...

...245), (-524, -502), (-781, -759), (-1038, -1016)). Negative range
    offsets are then adjusted modulo the **cache** size, giving the set of
    interval ranges to be avoided: ((65525, 65535), (0, 12), (65269...

00782252
Method and apparatus for instruction issue
Verfahren und Vorrichtung zur Befehlsausgabe
Procede et dispositif pour la delivrance d'instructions
PATENT ASSIGNEE:
  FUJITSU LIMITED, (211467), 1-1, Kamikodanaka 4-chome, Nakahara-ku,
    Kawasaki-shi, Kanagawa 211-8858, (JP), (Proprietor designated states:
    all)
INVENTOR:
  Shebanow, Michael C., 1920 Glenwood Drive, Plano, Texas 75075, (US)
  Gmuender, John, 2337 Vendale Avenue, San Jose , CA 95124, (US)
  Simone, Michael A., 925 Redwood Avenue, Sunnyvale, CA 94086, (US)
  Szeto, John R.F.S, 1217 E. 34th Street, Oakland, CA 94610, (US)
  Maruyama, Takumi, 20 East Main Street, No.30, Los Gatos, CA 95032, (US)
  Tovey, DeForest W., 14165 Old Japanese Road, Los Gatos, CA 95030, (US)
LEGAL REPRESENTATIVE:
  Liesegang, Roland, Dr.-Ing. (7741), FORRESTER & BOEHMERT
    Pettenkoferstrasse 20-22, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date):   EP 730224   A2   960904 (Basic)
                                EP 730224   A3   970528
                                EP 730224   B1   021009
APPLICATION (CC, No, Date):   EP 96103208 960301;
PRIORITY (CC, No, Date): US 397891 950303
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU;
  MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: G06F-009/38
ABSTRACT WORD COUNT: 123
NOTE:
  Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text   Language   Update   Word Count
        CLAIMS A   (English) EPAB96   717
        CLAIMS B   (English) 200241   953
        CLAIMS B   (German)   200241   922
        CLAIMS B   (French)   200241   978
        SPEC A   (English) EPAB96   6828
        SPEC B   (English) 200241   6719
Total word count - document A   7546
Total word count - document B   9572
Total word count - documents A + B   17118
...SPECIFICATION second-oldest-instruction selector 134. The
  second-oldest-instruction selector 134 provides a 1-hot **second**
  -oldest-instruction **vector** 136- **2** (EX2(0,...,7)) to the instruction
  queue 116. The instruction vectors 136 are **1 - hot   vectors** , i.e. at
  most one bit may be set. In response to the instruction vectors...two
  entries from the current cycle eligible entries vector 526
  (RNEW(0,...,7)) and provides **1 - hot** oldest-instruction **vector** 537
  (EX1(underscore)NEW(0,...,7)) and a 1-hot **second** -oldest-instruction
  vector 539 (EX2(underscore)NEW (0,...,7)). The instruction selector 540
  selects the instructions from the...

...SPECIFICATION second-oldest-instruction selector 134. The
  second-oldest-instruction selector 134 provides a 1-hot **second**
  -oldest-instruction **vector** 136- **2** (EX2(0,...,7)) to the instruction
  queue 116. The instruction vectors 136 are **1 - hot   vectors** , i.e. at
  most one bit may be set. In response to the instruction vectors...two
  entries from the current cycle eligible entries vector 526
  (RNEW(0,...,7)) and provides **1 - hot** oldest-instruction **vector** 537
  (EX1(underscore)NEW(0,...,7)) and a 1-hot **second** -oldest-instruction
  vector 539 (EX2(underscore)NEW (0,...,7)). The instruction selector 540
  selects the instructions from the...

15/3,K/10   (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01134900   **Image available**
PAGE DESCRIPTORS FOR PREFETCHING AND MEMORY MANAGEMENT
DESCRIPTEURS DE PAGE POUR GESTION DE LECTURE ANTICIPEE ET DE MEMOIRE
Patent Applicant/Assignee:
   INTERNATIONAL BUSINESS MACHINES CORPORATION, New Orchard Road, Armonk, NY
      10504, US, US (Residence), US (Nationality)
   IBM UNITED KINGDOM LIMITED, PO Box 41, North Harbour, Portsmouth,
      Hampshire PO6 3AU, GB, GB (Residence), GB (Nationality), (Designated
      only for: MG)
Inventor(s):
   FRANASZEK Peter, 12 Spring Glen Drive, Mount Kisco, NY 10549, US,
Legal Representative:
   LITHERLAND David Peter (agent), IBM United Kingdom Limited, Intellectual
      Property Law, Hursley Park, Winchester, Hampshire SO21 2JN, GB,
Patent and Priority Information (Country, Number, Date):
   Patent: WO 200457479 A2 20040708 (WO 0457479)
   Application: WO 2003GB5401 20031211 (PCT/WO GB03005401)
   Priority Application: US 2002326634 20021220
Designated States:
(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)
   AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
   DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
   LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU
   SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
   (EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
   SI SK TR
   (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
   (AP) BW GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
   (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 5160

Fulltext Availability:
   Detailed Description

Detailed Description
... associated selected tag prefetched from the main memory, and updating
   the information associated with this **tag** and page into the main memory.

   Also, the method step of accessing the tag in...
...to a page, on the
   tag, wherein the tag includes at least a first and **second** history
   vectors ,
   and denoting an ith bit of the at least **first** and **second**   **vectors** to
   determine whether a line corresponding to the tag in the prefetch buffer
   was accessed...

...cache lines.

   Preferably the present invention provides a computer system further
   comprising updates and/or **modifications** of the tags by the system
   software.

   Preferably the present invention provides a computer system...

...to a page, on the tag, wherein the tag includes
   at least a first and **second** history **vectors** ; and denoting an ith bit
   of
   the at least **first** and **second**   **vectors** to determine whether a line
   corresponding to the tag in the prefetch buffer was accessed...

...information on the first vector further comprises the step of: entering a one for each **cache** line referenced during the latest visit of the tag.

Preferably the present invention provides for...

15/3,K/36   (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00939749   **Image available**
**WIRELESS   COMMUNICATIONS METHODS AND SYSTEMS FOR LONG-CODE AND OTHER SPREAD
    SPECTRUM WAVEFORM PROCESSING**
**SYSTEMES   ET   PROCEDES   DE   COMMUNICATIONS   SANS   FIL POUR LE TRAITEMENT DE
    FORMES D'ONDE A ETALEMENT DU SPECTRE ET DE FORMES D'ONDE LONG CODE**
Patent Applicant/Assignee:
  MERCURY COMPUTER SYSTEMS INC, 199 Riverneck Road, Chelmsford, MA 01824,
    US, US (Residence), US (Nationality)
Inventor(s):
  OATES John H, 59B Seaverns Bridge Road, Amherst, NH 03031, US,
Legal Representative:
  POWSNER David J (et al) (agent), Nutter, McClennen & Fish LLP, One
    International Place, Boston, MA 02110-2699, US,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200273937 A2-A3 20020919 (WO 0273937)
  Application: WO 2002US8106 20020314   (PCT/WO US0208106)
  Priority Application: US 2001275846 20010314; US 2001289600 20010507; US
    2001295060 20010601
Designated States:
(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)
  AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
  EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS
  LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ
  TM TR TT TZ UA UG UZ VN YU ZA ZW
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 149462

Fulltext Availability:
  Detailed Description

Detailed Description
... matched-filter outnuts can be re-written.

  31
  Y (kqn+l) [M] + A (0)
  YA(**n** +l)
  I jr rlq Clni
  2N, **n** = O   [nN, +MTJ In]
  1 **N** , - **1**
  YA(**n**)
  r, [nN, 4-i"') +mT]. In]
  Iq I CIm
  2NI n=0
  Ni-I A...

15/3,K/46   (Item 37 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR DEVICE, OPERATING SYSTEM,
    AND NETWORK TRANSPORT NEUTRAL SECURE INTERACTIVE MULTI-MEDIA MESSAGING
SYSTEME, PROCEDE ET PRODUIT PROGRAMME D'ORDINATEUR POUR APPAREIL, SYSTEME
    D'EXPLOITATION ET MESSAGERIE MULTIMEDIA INTERACTIVE RESEAU, NEUTRE ET
    SECURISEE

Inventor(s):
  ILLOWSKY Daniel H, 21363 Dexter, Cuptertino, CA 95014, US,
  WENOCUR Michael L, 4057 Amaranta Avenue, Palo Alto, CA 94306, US,
  BALDWIN Robert W, 990 Amarillo Avenue, Palo Alto, CA 94303, US,
  SAXBY David B, 14946 Granite Court, Saratoga, CA 95070, US,
Legal Representative:
  ANANIAN R Michael (et al) (agent), Flehr Hohbach Test Albritton & Herbert
    LLP, 4 Embarcadero Center, Suite 3400, San Francisco, CA 94111-4187, US
    ,

Fulltext Availability:
  Detailed Description

Detailed Description
... Client's digital certificate, or other information sent by the Client
  before sending the Message **Tag** .

  The SHA1 digest function shown above can be replaced with any
  cryptographically secure compression or...

...MAC, 3DES-CBC-MAC, IDEA-CBC-MAC, AES-CBC-MAC, DES-MDC, and DES-MDC2.

  1   2 Creating of Message **Tags**
  110 The-following algorithm creeftes'Message' **Tags** from Message [Ds. It
  is shown operating on 12-byte (96-bit) values, though it...

Set	Items	Description
S1	0	((1 OR ONE OR 1ST OR FIRST)()HOT)(2W)(VECTOR? ? OR TAG? ? - OR FLAG? ? OR INDICATOR? ?)
S2	26163	(1 OR ONE OR 1ST OR FIRST)(2N)VECTOR? ?
S3	42780	(N(1W)1 OR N()MINUS()(1 OR ONE))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S4	0	((2 OR TWO OR 2ND OR SECOND???)()HOT)(2W)(VECTOR? ? OR TAG? ? OR FLAG? ? OR INDICATOR? ?)
S5	30148	(2 OR TWO OR 2ND OR SECOND??)(2N)VECTOR? ?
S6	56756	(N(1W)2 OR N()MINUS()(2 OR TWO))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S7	276	(NBIT OR N()BIT)(2W)(STRING? ? OR BLOCK? ? OR FRAGMENT? ? - OR WORD? ? OR STATEMENT? ?)
S8	131617	TAG? ? OR TLB OR TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()- BUFFER? ? OR CACH???
S9	255	S2:S3(10N)S5:S6(10N)(CONVERT??? OR CONVERSION? ? OR TRANSF- ORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERATION? ? OR MODIF???? OR MODIFICATION)
S10	1	S7:S8 AND S9
S11	61	S3(10N)S6(10N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERA- TION? ? OR MODIF???? OR MODIFICATION)
S12	57	RD (unique items)
S13	193	S2(10N)S5(10N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERA- TION? ? OR MODIF???? OR MODIFICATION)
S14	57	S10 OR S12

14/5/37   (Item 2 from file: 239)

02656426 MR 97c#94002
Wavelet transform for time-frequency representation and filtration of discrete signals.
Popinski, W.
Appl. Math. (Warsaw)
Language: English   Summary Language: English
Document Type: Journal
Journal Announcement: 9611
Subfile: MR (Mathematical Reviews) AMS
Abstract Length: MEDIUM (11 lines)
Summary: ``We present a method for analysing and filtering real-valued discrete signals of finite duration $s(n),\ n = 0 , 1 ,\cdots,N-1$, where $ N = 2 \sp p,\ p> 0 $, by means of time-frequency representation. This is achieved by defining an invertible discrete **transform** representing a signal either in the time or in the time-frequency domain, which is based on decomposition of a signal with respect to a system of basic orthonormal discrete wavelet functions. Such discrete wavelet functions are defined using the Meyer generating wavelet spectrum and the classical discrete Fourier transform between the time and the frequency domains.''
Reviewer: Summary
Review Type: Abstract
Descriptors: *94A12 -Information and communication, circuits-Communication, information-Signal theory (characterization, reconstruction, etc.) ; 42C15 -Fourier analysis-Nontrigonometric Fourier analysis-Series of general orthogonal functions, generalized Fourier expansions, nonorthogonal expansions

14/5/56   (Item 21 from file: 239)

01057025 MR 15,163a
Tables of coefficients for the numerical calculation of Laplace transforms.
Salzer, Herbert E.
Publ: U. S. Government Printing Office, Washington 25, D. C.
no year given., ii+36 pp.
Series: National Bureau of Standards Applied Mathematics Series, No. 30.
Language: English
Document Type: Book
Subfile: MR (Mathematical Reviews) AMS
Abstract Length: LONG (31 lines)
This pamphlet is concerned with the approximate numerical evaluation of integrals of the form $$ \int\sb 0\sp \infty e\sp {-pt}f(t)\,dt \ \tag $\ast$ $$ as a sum of the form $\sum\sb {i=0}\sp {n-1}A\sb i{}\sp {(n)}(p)f(i)$. The formula can be made exact, by suitable choice of the $A\sb i$, if $f(i)$ is a polynomial of degree not exceeding $n-1$; otherwise its accuracy depends on the accuracy with which $f(t)$ may be approximated by such a polynomial. The tables are designed for use when $f(t)$ is replaced by a Lagrange interpolation polynomial of degree $n-1$ for $t=0(1)n-1$. Examples of the use of the tables and of the determination of error estimates are given.
    The tables themselves are as follows. Schedule A: Lagrange interpolation coefficients. This gives $L\sb i{}\sp {(n)}(t)$ defined by the approximate formula $$ f(t)\doteqdot\sum\sb {i=0}\sp {n-1}L\sb i{}\sp {(n)}(t)f(i)/(n-1)! $$ as polynomials in t for $ n = 2 (1)11$, $i= 0 (1)n-1$. Schedule B: Laplace **transforms** of interpolation coefficients. This gives coefficients $B\sb i{}\sp {(n)}(p)$ as polynomials in p, for the same ranges of n and i, where $p\sp nB\sb i{}\sp {(n)}(p)(n-1)!$ is given by $(*)$ when $f(t)$ is the Lagrange coefficient $L\sb i{}\sp {(n)}(t)/(n-1)!$. The polynomials in the second schedule may be obtained

from those in the first by replacing $t\sp r$ by $r!p\sp {n-r-1}$.

Table I gives 8 decimal (or 8 figure) numerical values of $A\sb i{}\sp {(n)}(p)$ for $ n = 2 (1)11$, $i= 0 (1)n-1$, and for $$ \align p & =0.1(0.1)n-1\quad\text{to}\quad n=7\\ p & =0.2(0.2)n-1\quad\text{to}\quad n=9\\ p & =\quad 1(1)n-1\quad\ \ \text{to}\quad n=11. \endalign $$

Table II gives 9 figure values of $n!/p\sp {n+1}$ for $n=0(1)10$, $p=0.1(0.1)10$.

It is a pity to have to comment that the arrangement of the tables leaves very much to be desired.

Reviewer: Miller, J. C. P.

Review Type: Signed review

Descriptors: *65.0X -Numerical analysis

14/5/57 **(Item 22 from file: 239)**

01034447 MR 11,585g

Simple construction of generalized Peano curve.

Iseki, Kiyosi

J. Osaka Inst. Sci. Tech. Part I.

1949,   1,,   1--2

Language: English

Document Type: Journal

Subfile: MR (Mathematical Reviews)   AMS

Abstract Length: SHORT (9 lines)

Modifying a method by Lebesgue, the author gives the following example of a Peano curve $x\sb n=\phi\sb n(t)$ ($ n = 1 , 2 ,3,\cdots$; $ 0 \leq t\leq 1$) passing through all points of Hilbert space satisfying $0\leq x\sb n\leq 1$: $$ \phi\sb n(t)=\sum\sb {k=1}\sp \infty2\sp {-k}f(3\sp {2\sp {n-1}-1+2\sp n(k-1)}t), $$ where $f(t)$ is defined for $t\geq 0$, continuous, and $$ f(t)=\cases 0,\quad 2m-{\textstyle\frac 1{3}}\leq t\leq 2m+{\textstyle\frac 1{3}},\\ 1,\quad 2m+{\textstyle\frac 2{3}}\leq t\leq 2m-{\textstyle\frac 4{3}}. \endcases $$

Set	Items	Description
S1	0	((1 OR ONE OR 1ST OR FIRST)()HOT)(2W)(VECTOR? ? OR TAG? ? - OR FLAG? ? OR INDICATOR? ?)
S2	5853	(1 OR ONE OR 1ST OR FIRST)(2N)VECTOR? ?
S3	3643	(N(1W)1 OR N()MINUS()(1 OR ONE))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S4	0	((2 OR TWO OR 2ND OR SECOND???)()HOT)(2W)(VECTOR? ? OR TAG? ? OR FLAG? ? OR INDICATOR? ?)
S5	5454	(2 OR TWO OR 2ND OR SECOND??)(2N)VECTOR? ?
S6	3058	(N(1W)2 OR N()MINUS()(2 OR TWO))(3W)(ZERO?? OR O OR 0 OR OS OR 0S)
S7	21	(NBIT OR N()BIT)(2W)(STRING? ? OR BLOCK? ? OR FRAGMENT? ? - OR WORD? ? OR STATEMENT? ?)
S8	435572	TAG? ? OR TLB OR TRANSLATION()(LOOKASIDE OR LOOK()ASIDE)()- BUFFER? ? OR CACH???
S9	1143	S2:S3(20N)S5:S6
S10	9	S9(50N)S7:S8
S11	761	S2(20N)S5
S12	384	S3(20N)S6
S13	22	S3(20N)S6(20N)(CONVERT??? OR CONVERSION? ? OR TRANSFORM??? OR TRANSLAT???? OR BRIDG??? OR CHANG??? OR ALTER??? OR ALTERA-TION? ? OR MODIF???? OR MODIFICATION)
S14	31	S10 OR S13
S15	25	RD (unique items)

15/3,K/1   (Item 1 from file: 275)

01497061   SUPPLIER NUMBER: 11744990   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Hewlett-Packard debuts low-end RISC stations. (HP 705 and 710
  reduced-instruction-set computer workstations) (Product Announcement)**
Stedman, Craig
Electronic News (1991), v38, n1894, p13(2)
Jan 13, 1992
DOCUMENT TYPE: Product Announcement   ISSN: 1061-6624   LANGUAGE:
  ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1046   LINE COUNT: 00079

...   use the same CPU. However, HP hopes the 720 will be protected by
its greater **cache** and higher memory, storage and graphics capacities.
      The company, which is formally unveiling the 705...

...array that increases their maximum storage capacity to 236GB. Two
24-plane graphics boards, with **1 .15 million** **vectors** per **second**
drawing speed, are also being introduced for the model 720 and above.

15/3,K/2   (Item 1 from file: 16)

10563031   Supplier Number: 104258717   (USE FORMAT 7 FOR FULLTEXT)
Mutual Funds.
National Post, v5, n188, pIN14(6)
June 7, 2003
Language: English   Record Type: Fulltext
Document Type: Newspaper; Trade
Word Count: 38821

...   Eq Value   FR -0.07

                  Optimum Investments Inc(n)

      22.02   19.79   Balanced   Y * **N**   0
.03
      13.56   13.01   Bonds   Y * N   0.01
      13.17   10.31   Equity...

15/3,K/3   (Item 2 from file: 16)

02915882   Supplier Number: 43937332   (USE FORMAT 7 FOR FULLTEXT)
Comparison of Stress Measurement Techniques
Glass, p268
July, 1993
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1189

...   glass is 2.65 Brewster (one Brewster unit is $10(-12)m(2)/N$), the
change in index becomes:
      $n (1) - n (2) = 0 .000265$, at 100MPa surface stress
    This small index **change** cannot be resolved with satisfactory
precision and so surface stresses in heat-strengthened materials should...

15/3,K/4   (Item 3 from file: 16)

02667646   Supplier Number: 43556419 (USE FORMAT 7 FOR FULLTEXT)
CRACKERS: FIGHTING BACK
Snack Food, v0, n0, p30
Jan, 1993
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3750

...   4   -5.0

FLAKED SODA	Retail Sales	$356,694	$417,204	$427,065	$406,995
	% Change	N/A	17.0	2.4	-4.7
	Lb Volume	343,974	358,509	357,745	342,600
	% Change	N/A	4.2	-0.2	-4.2
SPRAYED BUTTER	Retail Sales	$384,876	$391,627	$379,806	$361,240
	% Change	N /A	1 .8	-3. 0	
-4.9					
	Lb Volume	178,998	173,386	163,138	154,634
	% Change	N/A	-3.1	-5.9	-5.2
CHEESE	Retail Sales	$238,300	$244,226	266,255	$291,267
	% Change	N /A	2 .5	9. 0	
9.4					
	Lb Volume	98,191	93,842	96,579	100,227
	% Change	N/A...			

15/3,K/5   (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

02316359   Supplier Number: 43033060 (USE FORMAT 7 FOR FULLTEXT)
European TPE use to rise at 6%
European Rubber Journal, p27
June, 1992
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 548

...   5   1   2   1   0   9

Footwear	47	0	0	7	1	1	56
Polymer **modifier**	11	3	3	n	n	n	18
Hose/tubes	0	2	2	2.5	1...		

...5

Mechanical goods	1	6.5	5	4.5	1.5	1	19.5
Bitumen **modifier**	30	0	0	0	0	0	30
Construction	n	0		2 .5	n	0	0
3							
Adhesives/coating	16	0	0	11	n	n	27
Film/sheet	0	0	0	1	**n**	0	1
Other	5	n	n	n	2	n	8
Total	117	79	20	31	8	5...	

15/3,K/6   (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

02060974   Supplier Number: 42663205 (USE FORMAT 7 FOR FULLTEXT)
Hewlett-Packard Debuts Low-End RISC Stations
Electronic News (1991), p13
Jan 13, 1992
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1000

...   use the same CPU. However, HP hopes the 720 will be protected by its greater **cache** and higher memory, storage and graphics capacities.
The company, which is formally unveiling the 705...array that increases their maximum storage capacity to 236GB. Two 24-plane graphics boards, with **1** .15 million **vectors** per **second** drawing speed, are also being introduced for the model 720 and above.

15/3,K/7   (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

01236716   Supplier Number: 41431998   (USE FORMAT 7 FOR FULLTEXT)
Sparc server packs supercomputer punch
Electronic Engineering Times, p1
July 9, 1990
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 820

...   vector processor can sustain this peak performance in certain circumstances through the use of a **1** -Mbyte **vector   cache** that is linked to the **vector** processor by **two** output and one input ports. The ports provide an aggregate bandwidth of 1.28 Gbytes...

...performing a mixed triadic operation involving an add and a multiply, and when there are **two   vector** inputs and **one** scalar input, explained Carlton Jeffcoat, director of product marketing for distributed computing products. Entire arrays can be moved into **cache** and operated on by the vector processor, obviating the usual need to break down the...

15/3,K/8   (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

16375671   SUPPLIER NUMBER: 106514686   (USE FORMAT 7 OR 9 FOR FULL TEXT
)
U.S. international transactions, first quarter 2003.
Weinberg, Douglas B.; Abaroa, Patricia E.
Survey of Current Business, 83, 7, 49(65)
July, 2003
ISSN: 0039-6222   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 77595   LINE COUNT: 27987

...   2.4   -5.3
          Nonpetroleum products   0.5   -4.3   3.9   2.1

                                  Percent **change** from
                                    previous period
                                  (chained (1996) dollars)

                                              2003

                              II   III   IV   I (p)

     Exports   3.1...
...6
          Agricultural poducts   -2.6   -4.8   -0.4   2.8
          Nonagricultural products 3.6   **1** .3   -2.4   0 .4

     Imports   5.1   1.0   1.6   -0.8
          Petroleum and products   7.9...

15/3,K/9   (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

15636164   SUPPLIER NUMBER: 99130107   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Toronto stock exchange. (Investing).
National Post, 5, 99, IN5(4)
Feb 22, 2003
ISSN: 1493-4779   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 36097   LINE COUNT: 16430

```
...      TSX  C              TCF
                      26.84    18.88    TD TSX                TTF
                       9.65     5.50    TDCdnGrwth            TAG
                      29.74    10.76    TDSpltCap             TDS
                      15.59    14.80    TDSpit pf
             (down arrow) 1...TELUS Gpf
                      20.65     5.76    TELUS
                      19.20     5.56    TELUS nv **
           (up arrow) n   1 .30     0 .70      TGS Ppty
                TSL
                       5.98     1.28    TLC Vision
           TLC
                       7.50     4.75...
```


 15/3,K/10   **(Item 3 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB

14721705   SUPPLIER NUMBER: 87914940   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Toronto Stock Exchange 06.07.02. (Investing).
National Post, 4, 190, IN11(2)
June 8, 2002
ISSN: 1493-4779   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 19759   LINE COUNT: 12879

```
...      70      eNGENTY              -         -
                      11.20     7.30    Enghouse #           -      16.4
                      18.40    10.25    EnsignRes #      1. 2       14
.2
                       7.50     3.00    EnSource             -      33.7
                       4.17     0.50    EnvoyCom #           -        -
                       1.44...
```


 15/3,K/11   **(Item 4 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB

14537872   SUPPLIER NUMBER: 85250418   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mutual Funds 04.12.02. (Investing).
National Post, 4, 142, IN5(6)
April 13, 2002
ISSN: 1493-4779   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 41237   LINE COUNT: 13561

```
...      Income                  (*) N

5.26                        3.38    Japanese                     N
     9.73                   7.26    RSP Gbl Divers               (*)
N

7.88                        5.03    RSP Japanese              (*) N

10.41                      10.21    ST Cdn Inc               (*) N
     12.01                 10.96    ST Gbl Inc                   (*)
N

5.76                        5.33    ST Govt Bond             (*) N
```

```
 46.01                        31.73   Select Amer                    N
     22.45                        16.03   Special Growth                 (*)
N
     23.66                        15.70   US Larger Co
N


     Altamira Sector


 9.80                          7.03   Biotechnology                    N
     13.75                        10.16   Glob Finl Serv...
```

15/3,K/12   (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

13907301   SUPPLIER NUMBER: 78864239   (USE FORMAT 7 OR 9 FOR FULL TEXT)
National Income and Product Accounts Tables.(Statistical Data Included)
Survey of Current Business, 81, 8, 34
August, 2001
DOCUMENT TYPE: Statistical Data Included   ISSN: 0039-6222
LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 41884   LINE COUNT: 18607

```
...       2      681.3      713.1
               tax and nontax
               liability
          Business transfer      14       36.8      38. 0        41.3
               payments
          Statistical            15       29.7     -31. 0       -72.7
               discrepancy
     Plus: Subsidies less        16       19.1      23.5        33.3
               current surplus...
```

15/3,K/13   (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

13800192   SUPPLIER NUMBER: 77830936   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**THE CYCLICALITY OF REAL WAGES WITHIN EMPLOYER-EMPLOYEE MATCHES.(Statistical
  Data Included)**
DEVEREUX, PAUL J.
Industrial and Labor Relations Review, 54, 4, 835
July, 2001
DOCUMENT TYPE: Statistical Data Included   ISSN: 0019-7939
LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 8899   LINE COUNT: 00871

...   Wage and Earnings
     Cyclicality of Workers Who were
     Not Salaried or Hourly and Did
     Not **Change** Employer, 1976-77 to
     1990-91. a
     (Standard Errors in Parentheses)

	Mean Regression	
	Hourly	Earnings Divided by
Sample (Sample Size)	Wage	Hours
All Job Stayers (1,539)	**N** /A	- **2** .17 **
		(**0** .97)
Stayers with No Extra Jobs (1,244)	**N** /A	- **1** .12
		(**0** .96)

	Median Regression	
	Earnings	Hourly Wage
Sample (Sample Size)	Earnings	Wage

15/3,K/14   (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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13393251   SUPPLIER NUMBER: 68876761   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Crises, Contagion, and the Closed-End Country Fund Puzzle.
LEVY-YEYATI, EDUARDO; UBIDE, ANGEL
International Monetary Fund Staff Papers, 47, 1, 54
March, 2000
ISSN: 0020-8027   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 10821   LINE COUNT: 00882

...   in equations (6) and (7), one can readily see that
$dDIS/dSTR = (p'._{sub.1}) - (n'._{sub. 1})$ (less than) **0** ,
$dDIS/dMSCI = (p'._{sub.2}) - (n'._{sub. 2})$ (greater than) **0** .
     (33.) Note that, although it was reasonable to expect Asian II
countries to suffer spillovers on fundamentals (e.g., a deterioration of
the current account),the se fundamental **changes** should have had he same
effect on fund prices and NAV, with no impact on...

15/3,K/15   (Item 8 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

11900382   SUPPLIER NUMBER: 60903572   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Genetic Susceptibility and Survival: Application to Breast Cancer.
JR., EDWIN S. IVERSEN; PARMIGIANI, GIOVANNI; BERRY, DONALD A.; SCHILDKRAUT,
JOELLEN M.
Journal of the American Statistical Association, 95, 449, 28
March, 2000
ISSN: 0162-1459   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 11898   LINE COUNT: 01006

...   BRCA1-radiation treatment interaction term, and the BRCA2-radiation
treatment interaction term. For these parameters, **N (0 , 1)**, **N (0 , (**
2 .sup.2)), N(**0** , (5.sup.2)), and N(0, (10.sup.2)) densities are
specified.
     The effect on the distribution of the BRCA2 coefficient of **changing**
the prior is to shorten its left tail, leaving its right tail virtually
unchanged. In...

15/3,K/16   (Item 9 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

10167173   SUPPLIER NUMBER: 20234328   (USE FORMAT 7 OR 9 FOR FULL TEXT)
A microwave radial power combiner design.
Rheem, Jae-Wook; Kang, Won-Tae; Lee, Sang-Ho; Kim, Duk-Yong; Chang, Ik-Soo
Microwave Journal, v40, n11, p22(7)
Nov, 1997
ISSN: 0192-6225   LANGUAGE: English   RECORD TYPE: Fulltext
WORD COUNT: 2146   LINE COUNT: 00182

...   4, (R.sub.o) = 50 (ohms). However, considering that the four-way
structure can be **changed** to a three-way structure in this design, the
characteristic impedance of the (Lambda)/4...

...to be 93 (ohms) using
     $(Z._{sub.o}) = ((\text{square root of } n) + (\text{square root of } n - 1)/ 2$
)(R.sub. **o**) (21)
     where
     n=4
     (R.sub.o) = 50 (ohms)

The four-way radial power combiner...

15/3,K/17   (Item 10 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09656767   SUPPLIER NUMBER: 19321007   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Another look at the salamander mating data: a modified Laplace
   approximation approach.**
Shun, Zhenming
Journal of the American Statistical Association, v92, n437, p341(9)
March, 1997
ISSN: 0162-1459   LANGUAGE: English   RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5261   LINE COUNT: 00513

...   This implies that the correction term for the approximation should
have an exponentiated form. A **modified** approximation derived by Shun and
McCullagh (1994) is the standard Laplace approximation multiplied by an...

...sub.a), ((Sigma).sub.b)) (varies) ((det(H.sub.0)).sup.-1/2)(e.sup.-(**n**
.sup. **2**)(Phi)((x.sub. **0**))) x exp{(R.sub. **n**) + **O** (**1** /n)}, (7)
      where (R.sub.n) is (R.sub.(Lambda)) in (2). The relative error...

...O(1/n), the square root of the sample size. The following example
illustrates the **modified** approximation.
      Example 1. As previously noted, (Phi) depends on the average of the
conditional log...

15/3,K/18   (Item 11 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07620128   SUPPLIER NUMBER: 16502929   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Framework for the analysis of pension and unemployment benefit reform in
   Poland.**
Perraudin, William; Pujol, Thierry
International Monetary Fund Staff Papers, v41, n4, p643(32)
Dec, 1994
ISSN: 0020-8027   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 9820   LINE COUNT: 00810

...   year retirement period.
      Table 6. A Measure of the Distortionary Impact of Pensions

r - v - n	- 2 %	- 1 %	0 %	1%	2%
g	1.67	1.30	1.00	0.76	0.43

      In what...

...condition holds. In Section II, we argued that the Polish labor force is
unlikely to **change** dramatically. Hence, whether or not the neutrality
condition holds depends on the relative magnitude of...

15/3,K/19   (Item 12 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07269693   SUPPLIER NUMBER: 15252727   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Beyond vectorizing compilers: the Standard Math Library.
Mirkin, Leo; LeBlanc, Michael; Inamdar, Rajendra
Defense Electronics, v26, n5, p25(4)
May, 1994
ISSN: 0278-3479   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2229   LINE COUNT: 00199

...   another set of standard vector and matrix operations called the

Basic Linear Algebra Subprograms (BLAS) [**1** , **2**]. These **vector** and matrix functions assume operands in memory and that results are returned to memory. The calls make no explicit reference to architecture dependent features such as **cache** or strip mining. Each vector operand is specified by its starting address and the distance...

15/3,K/20 **(Item 13 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB

06508526 SUPPLIER NUMBER: 14377757 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Daily exchange rate variance.
Harvey, John T.
Journal of Post Keynesian Economics, v15, n4, p515(26)
Summer, 1993
ISSN: 0160-3477 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 8537 LINE COUNT: 00671

... and this is not inconsistent with this model.
Table 8

Impact of a one-unit **change** in the independent variables on the probability of each bias

Dep var	ANEWMP	ANEWBOCA	ANEWIND	ANEWOTH
$\|\|E.sup.e$ .sub.t+ **n** $= 2$ (Deutsche Mark bias)	0 .40	0 .31	0.80	0.50
$\|\|E.sup.e$ .sub.t+ **n** $= 1$ (no bias)	0 .33	0 .25	0.65	0.40
$\|\|E.sup.e$ .sub.t+n $= 0$	-0...			

15/3,K/21 **(Item 1 from file: 624)**
DIALOG(R)File 624:McGraw-Hill Publications

0226151
CONOCO CHANGES LUBE PRICES
Platts Oilgram Price Report June 12, 1990; Pg 6-A; Vol. 68, No. 113
Journal Code: POP ISSN: 0162-1292
Dateline: Houston 6/11
Word Count: 51 *Full text available in Formats 5, 7 and 9*

TEXT:
Eff today Conoco has **changed** the following lube base oil prices: Cts/gal 90 S.N. and 100 S.N. unchanged, 150 S.N up 2. **0** , 200-250 S. **N** . up **2** . **0** , 300-325 S.N. up 2.00, 350 S. **N** . up **2** . **0** , 500 S. **N** , up **1** . **0** , 600 S. **N** . up **1** . **0** , 650 S. **N** . up **1** . **0** . and bright stock up 2.0.

15/3,K/22 **(Item 2 from file: 624)**
DIALOG(R)File 624:McGraw-Hill Publications

0156000
CITGO REVISES LUBE OIL BASE PRICES
Platts Oilgram Price Report August 18, 1989; Pg 3-A; Vol. 67, No. 159
Journal Code: POP ISSN: 0162-1292

TEXT:
... some of its posted prices for lube oil base stocks, but left others unchanged. The **changes** are: 90 and 100 Solvent Neutrals- both unchanged at 92.0 cts gal; 150 S. **N** . - down **1** . **0** ct to 91.0 cts gal; 200 S. **N** . - down **2** . **0** cts to 88.0 cts gal; 350 S.N. - down 3.0 cts gal to...

15/3,K/23   (Item 3 from file: 624)

0155918
EXXON REDUCES LUBE BASE STOCKS

TEXT:
... follows: Naphthenics - all (visc.) grades down 3.0 cts gal; Paraffinics - 100 S.N. - no **change** ; 150 S. **N** . - down **1** . **0** ct gal; 200/250 S. **N** . - down **2** . **0** cts; 300/350 S.N. - down 3.0 cts; 500 and 600 S.N. - no **changes** ; Bright stock - down 3.0 cts.

15/3,K/24   (Item 1 from file: 15)

02271936 86926326
Probabilistic analysis of a maintainable system with human error
B.S. Dhillon; Nianfu Yang

...TEXT: state j and has an elapsed repair time of x; for $j = m + n$, m + **n** + **1** , m + **n** + **0** **2**

N[sub]j(s) Laplace **transform** of N[sub]j(x).

Caption: Figure 1; . The state transition diagram of a general...

15/3,K/25   (Item 1 from file: 647)

00516427   CMP ACCESSION NUMBER: OST19920622S0579
Cray Intros First SPARC Product: `Superserver' Bridges SPARCs And
    Supercomputing Systems On Same Network
PAUL KRILL

...   Systems (FPS) server with reliability enhancements such as automatic parallelization detection in compilers and improved **caching** . Cray has purchased FPS.
       Cray said the S-MP will be used for what Cray...

...storage management and distributed graphics.

The S-MP has eight slots total for scalar and **vector** processors and **two** slots for parallel processors. Scalar processors take up **one** slot while **vector** processors take **two** .

Pricing starts at $500,000 for a unit one, 67-MIPS, Bipolar Integrated Technology scalar...